

Panelists Optimistic On Lower Power Design

One vendor told a conference this week that his firm can cut a device's power consumption by half, all with existing techniques and tools.

By Dylan McGrath, *EE Times*
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SAN JOSE, Calif. — Design for reduced power consumption may not be as daunting a challenge as widely assumed, according to a panel of industry executives here Thursday (Nov. 3) at Cadence Design Systems Inc.'s design chain partners event.

Gary Nacer, vice president of engineering at wireless device provider Sandbridge Technologies Inc. (White Plains, N.Y.), told the audience that his company has demonstrated the ability to reduce the power consumption of a device by 50 percent through the application of existing techniques and tools.

"High-performance, low-power consumption designs are achievable with current submicron processes," Nacer said.

Aurangzeb Khan, corporate vice president of market development at Cadence, said power challenges were "not something that cannot be overcome" by the industry.

Three of the four panelists were members of the Silicon Design Chain Consortium — a group that includes Cadence, ARM Ltd., Taiwan Semiconductor Manufacturing Co. (TSMC) and Applied Materials. The group recently created a low-power version of an ARM1136JS microprocessor chip that achieved an overall 40 percent reduction in power consumption compared to the standard version of the same chip.

Power is widely seen as the No. 1 concern of designers working on leading-edge designs. Though optimistic, panelists agreed there is plenty of room for improvement — and better tools, including for physical design, voltage islands, verification and timing and signal integrity analysis.

Robert Aitken, a senior architect at ARM, noted that there is a huge diversity of possible approaches to the power problem, and that all can be successful at some level.

"Everyone is looking at it from some different angle at the moment," Aitken said. "Over time, some will succeed and some won't."

Aitken said EDA tools that fit most easily into design flows, physical intellectual property (IP) that will adapt to suit market needs and cores that will adopt strategies that produce the best results would be most likely to succeed in the power market.

Invoking the spirit of the event, panelists (as well as the moderator, Professor Kurt Keutzer of the University of California, Berkeley) unanimously touted the importance of effective partnerships in overcoming power challenges.

"No one company can do it alone," said Ed Wan, senior director of design services marketing at TSMC. "It is important to pick the right partners."